Electrical Characterization of Analog Parameters of SOI MOSFET Devices and its Application as Current Mirror

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***Abstract* — Silicon-On-Insulator (SOI) technology has become an important alternative to sustain the continuous reduction of dimensions faced by conventional CMOS technology, due to improvements such as reduced junction capacitances and higher carriers mobility in the channel region, minimizing or delaying for more complex technological generations the occurrence of undesirable parasitic effects, such as short-channel effects. Besides, thin-film SOI transistors demonstrate excellent potential for analog applications. One of the most used blocks in analog circuits is the current mirror, which can be used both for the polarization of several branches of a circuit or to operate as an active load**

Keywords— Transistors, SOI MOSFET, Current mirror.

I. INTRODUCTION

The Silicon on Insulator (SOI) technology emerged as an alternative way for a conventional CMOS technology for the ultra-large-scale integration (ULSI). The presence of a film of insulator between the active area and the remaining substrate allows for a dielectric insulation between the devices, minimizing or eliminating the parasitic effects caused by the reduction of dimensions of MOS conventional technology [3].

The structure of a SOI MOSFET is presented in Fig.1. In this figure one can note that the transistor is fabricated in a thin film of silicon, placed in the top of a thick film of oxide. The buried oxide allows for the reduction in the parasitic effects when we compare to the conventional MOSFET devices, such as the latch-up effect. The presence of buried oxide also allows for lower parasitic capacitances.

In Figure 1, V_{GF} is the front gate voltage, V_{GB} is the back gate or substrate voltage, V_S is the source voltage and V_D is the drain voltage. The thickness of gate oxide (t_{oxf}), buried oxide (t_{oxb}), and Silicon layer (t_{Si}) are also indicated.

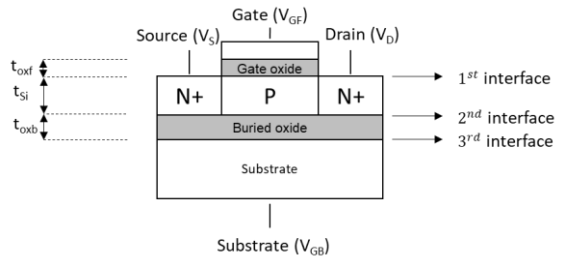

Figure 1 - Basic structure of SOI MOSFET

SOI transistor characteristics depends on the Si film thickness. If t_{Si} is thicker than twice the depletion depth, there is no interaction between the induced depletion region from the first and second interface and the device is named partially depleted. In the case where t_{Si} is smaller than the maximum depletion depth, certainly the depletion coming from first and second interfaces will touch each other and the silicon layer will be fully depleted for any gate bias higher than the threshold voltage (V_{TH}). These devices present the better characteristics among the SOI transistors and will be the focus of this study. SOI MOSFETs have a lot of advantages for analog applications, although they present reduced breakdown voltage. Current mirrors (CMs) are basic transistor stages of great importance for analog systems and can be used to bias or load analog circuit branches. In this analog block, the input current is mirrored to the output for any value of voltage applied to the drain of the output transistor [3].

In this work, an experimental analysis of analog parameters of SOI nMOSFETs will be analyzed. The drain current, transconductance, output conductance and intrinsic voltage gain will be presented. Also, the use of this transistor in a current mirror will be explored.

II. DEVICE CHARACTERISTICS AND MEASUREMENTS

The devices used in this work have been fabricated in a full depleted technology from UCLouvain [4], Belgium, with natural doping concentration of $10^{15}cm^{-3}$, t_{oxb} = 390 nm, t_{oxf} = 31 nm and t_{Si} = 80 nm. The channel presents doping concentration of $6x10^{16}$ cm^{-3}. Figure 2 shows the layout of chip used in this work. The set of devices present common source and gate and different drain pad. The channel width (W) of all devices is 20 µm and the channel length (L) of 0.75µm; 1.5 µm; 2 µm; 3 µm; 4 µm; 5 µm; 8 µm e 10 µm. The measured current mirror uses transistors with 2 µm of channel length and W= 20 µm [5].

Figure 2 – Layout of the chip used for electrical characterization.

Experimental curves have been obtained with a Keithley 4200 Semiconductor Characterization System, obtained at room temperature, with a Cascade Microtech Microprober.

III. Results and Analysis

A. Basic Electrical Parameters

In the Figure 3 have the experimental curves of drain current (I_D) as a function of gate-to-source voltage drop (V_{GS}) measured at V_{DS} = 1,50 V for different channel lengths. From these results, one can note that the drain current increases as the channel length decreases, which is in accordance with the first-order model described in the equations (1) and (2) for the triode and saturation modes, respectively:

$$I_{DS} = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH}) \cdot V_{DS} - \frac{1}{2} \cdot n \cdot V_{DS}^2 \quad (1)$$

$$I_{DS} = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{n \cdot L} \cdot (V_{GS} - V_{TH})^2 \quad (2)$$

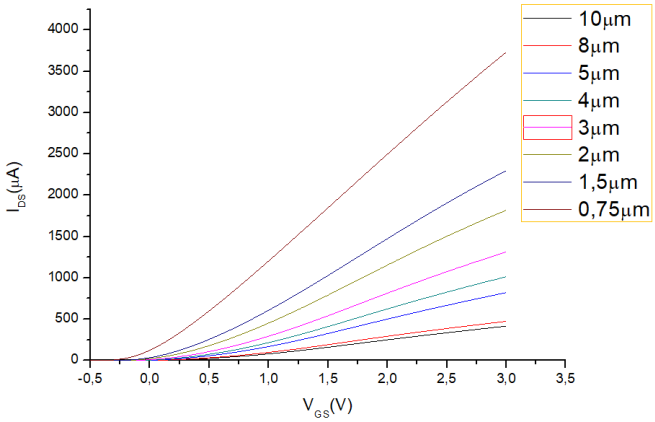

Figure 3 – Experimental I_{DS} x V_{GS} curve for different channel lengths, measured at V_{DS} = 1,5V

From these curves, basic electrical parameters have been extracted, as the threshold voltage, that is the second order derivative of the $\frac{\partial^2 I_{DS}}{\partial^2 V_{GF}}$.

Using the double-derivative method, the threshold voltage has been obtained and is presented as a function of the channel length in Figure 4. From these results, one can note the occurrence of short channel effect, responsible for the reduction in the threshold voltage because of the loss of the gate control. When L is reduced, the depletion regions of the source and drain, will be very significant compared to the induced depletion for the gate voltage. By this way, the depletion charge is controlled by the gate. We can detach that the thin film devices will suffer less influences because of the channel length [6,7].

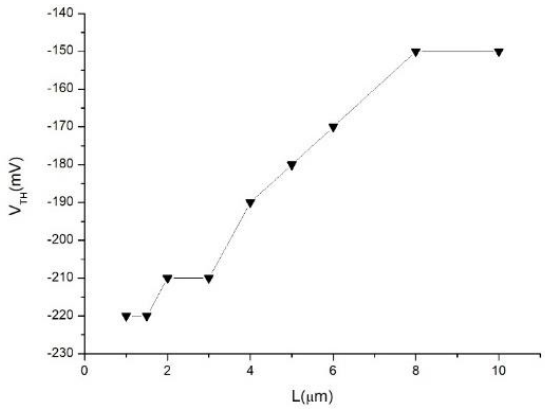

Figure 4 – Extracted threshold voltage as a function of channel length.

Another important basic parameter is the subthreshold slope (S), that express the gate voltage variation necessary to increase the I_{DS} in one order of magnitude [8]. The obtained results are presented in Figure 5. Once again, the occurrence of short-channel effects is seen for shorter devices, as an increase of subthreshold slope for L < 2 µm.

We can obtain this value using the relation using $\frac{dV_{GS}}{d(\log_{10}(I_{DS}))}$ using a low horizontal electrical field, in this case, 50 mV.

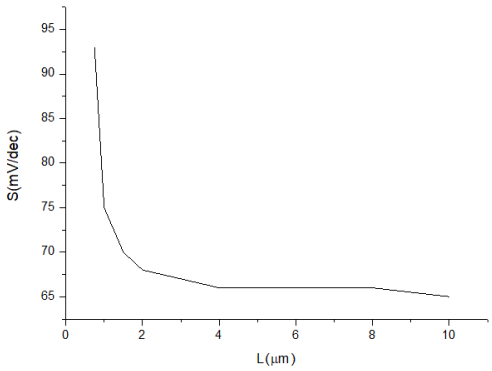

Figure 5 – Extracted subthreshold slope as a function of channel length.

B. Analog Parameters

Aiming at extracting analog parameters, I_{DS} x V_{GS} curves were also measured at V_{DS} = 1.5V. The current as a function of V_{DS} has been also obtained and is presented in Figure 6, with gate voltage overdrive, $V_{GT} = V_{GS} - V_{TH}$ = 200mV. Once again, the increase of current level is observed as the length is reduced.

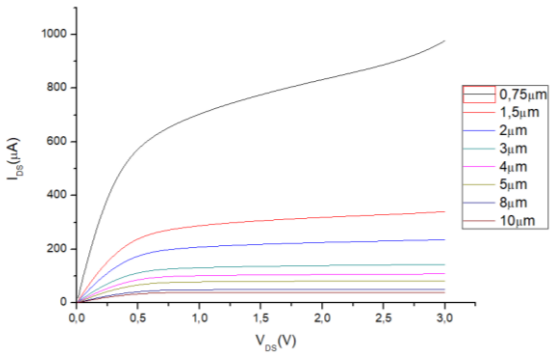

Figure 6 - Drain current x drain to source voltage graph

Aiming at analyzing a basic and one of the most important parameters of the measured devices, the transconductance ($g_m = dI_{DS}/dV_{GS}$) and the output conductance ($g_D = dI_{DS}/dV_{DS}$) are presented in Figure 7 and Figure 8, respectively, we can see that when the device suffer certain reduction of channel length L, the parasite effects can be increased, it results in a larger values for the gate and drain transconductance.

Analyzing this point, we can study the voltage gain using a relation between this information's.

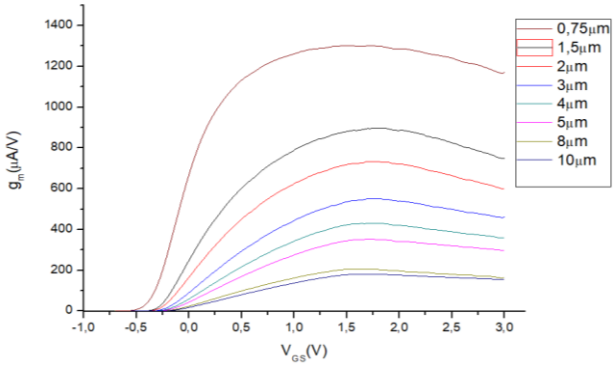

Figure 7 - Extracted transconductance as a function of gate voltage obtained at V_{DS} = 1.5V.

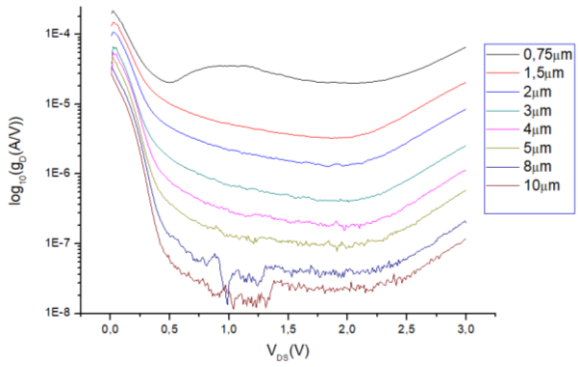

Figure 8 - Extracted output conductance as a function of drain voltage obtained at V_{GT} = 200 mV.

By combining the results of g_m and g_D, the intrinsic voltage gain is obtained ($A_V = g_m/g_D$) as shown in the Figure 9.

Doing the analysis it is possible to conclude that the g_D have a less increase than the gate transconductance g_m , it happens because the channel modulation, when your device become to be smaller, the early effect occurs with more ease, and, for consequence, voltage gain decreases.

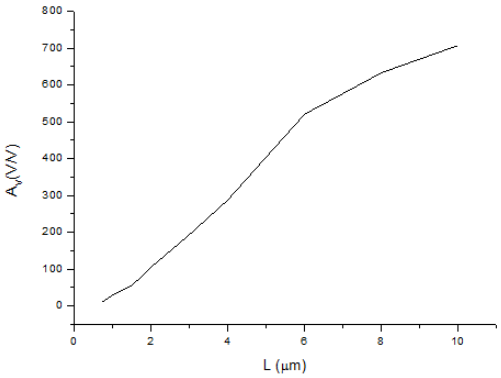

Figure 9 - Extracted intrinsic voltage gain as a function of channel length obtained at V_{GT} = 200 mV and V_{DS} = 1.5V.

C. *Current Mirror*

The current mirror, can be characterized by analog blocks, that can be used in the polarization of a many applications. The objective of the current mirror is to be a current sink, in other words, giving an output current proportionally to the input current.

The basic topology, named source-common current mirror can be seen in Figure 10. As in the measure current mirror, input and output transistor have the same dimensions, it is expected that $I_{DSout} = I_{DSin}$. However, due to the fabrication process, the two devices might be slightly different.

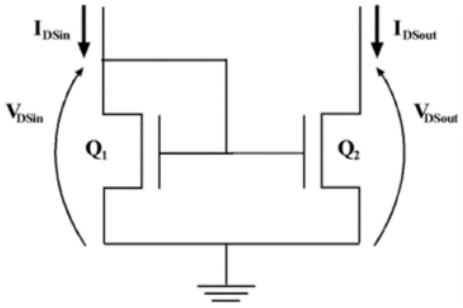

Figure 10 - Basic topology of current mirror

In order to verify the intrinsic mismatching between the two devices, the relation between the output and input current, named precision, $P = I_{DSout} / I_{DSin}$ has been measured fixing $V_{DSout} = V_{DSin}$ using a combination of two mosfets that have 2µm. The obtained result is presented in Figure 11, using a parameter called by V_{GT} of 200mV, this parameter can be understood by V_{GS}-V_{TH}. It is possible to see that P slightly deviates from unity even when there is no difference in bias conditions of input and output transistors.

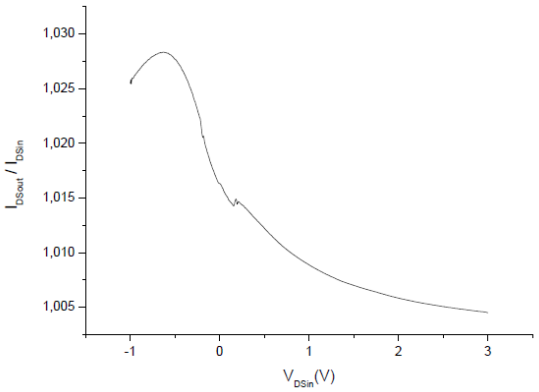

Figure 11 - Relation of the output and input current considering $V_{DSin} = V_{DSout}$.

Figure 12 presents the precision measured at different input current levels. One can note that, although the precision deviates from 1, the current is almost constant when the output transistor is in saturation.

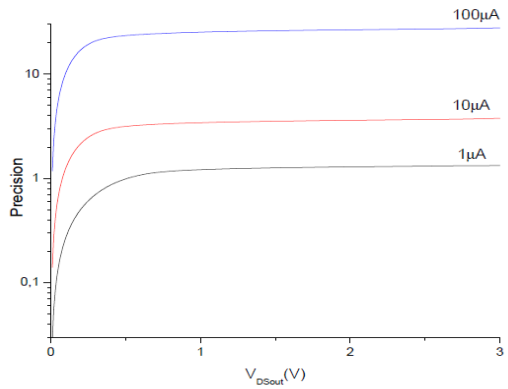

Figure 12 – Output current for fixed input current and varying output voltage.

After, in the Figure 13 presents the mirroring precision as a function of input voltage, measured at fixed output voltage of 1,5 V.

After the measures, it is possible to see that the precision does not occurs efficiently before the 1/3 of voltage applied in the output drain $V_{DS\ out}$, then, we can assume that the mirroring condition will not happen with any polarization condition.

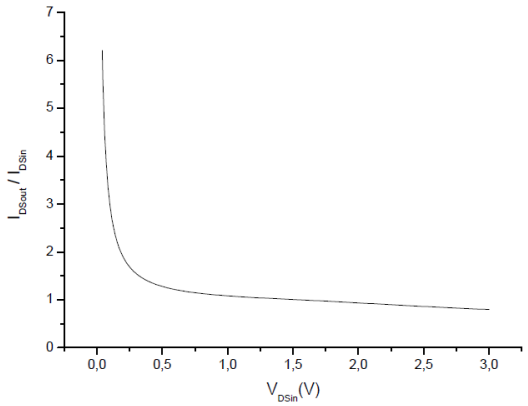

Figure 13 - Relation of the input and output transistor with the $\boldsymbol{V_{IN}}$ variation for the fixed $\boldsymbol{V_{DSout}}$ voltage.

IV. CONCLUSIONS

This work presented an experimental analysis of nMOS transistors with different channel lengths. From the measurements results and extracted parameters it has been observed that as the channel length is reduced short channel parasitic effects start to occur, and the threshold voltage become smaller. Also, at the same applied gate voltage overdrive short channel transistors can produce larger values of transconductance g_m and output conductance g_D, resulting in lower values for the intrinsic voltage gain.

A current mirror using SOI nMOSFETs have been also measured. It was possible to observe that even with the same V_{DS} at input and output, a small difference happens because the inherent differences in the devices. The precision is better at higher voltage bias, and the output resistance is high. Therefore, one can note that a possibility to use this as an active load, in fact, a resistor, with a larger value of resistances, using a smaller area of silicon.

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